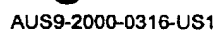


SECRET



OS
202

OS
204

OS
206

OS
208

Open Firmware
210

Kernel
212

Processor
232

Processor
234

Processor
236

Processor
238

I/O Adapter
248

I/O Adapter
250

Service Processor
290

Storage
270

NVRAM
298

I/O Adapter
252

I/O Adapter
254

Memory
240

Memory
242

Memory
244

Memory
246

I/O Adapter
256

I/O Adapter
258

I/O Adapter
260

I/O Adapter
262

Partitioned Hardware
230

200

Logically Partitioned Platform

AUS9-2000-0316-US1

The diagram illustrates a system architecture (300) with the following components and connections:

- Service Processor (302)**: Connected to the **SPCN/SN Table (324)** and the **SPCN Bus (380)**.
- SPCN/SN Table (324)**: Connected to the **Service Processor (302)** and **NVRAM (322)**.
- NVRAM (322)**: Connected to the **SPCN/SN Table (324)**.
- SPCN Bus (380)**: A central bus connecting the **Service Processor (302)** to the **I/O Drawers (304, 306, 308)** and the **Firmware (326)**.
- I/O Drawers (304, 306, 308)**: Each drawer contains two **PHB** components (310, 312; 314, 316; 318, 320).
- Firmware (326)**: Connected to the **SPCN Bus (380)**.
- System Memory (340)**: Contains the **OF Device Tree (342)** and is connected to the **SPCN Bus (380)**.

300
System
Figure 3
AU9-2000-0316-US1

Begin

Discover drawers.
502

Assign memory mapping to the drawer and its PHBs.
504

Create PHB nodes.
506

Create location codes for the PHB nodes.
508

**Update Open Firmware Device Tree in
system memory.**
510

```

graph TD
    Start([Start]) --> Input[Input]
    Input --> Process[Process]
    Process --> Output[Output]
    Output --> End([End])
  
```

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